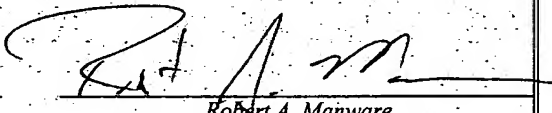


TRANSISTOR HAVING VERTICAL JUNCTION EDGE AND METHOD OF MANUFACTURING THE SAME

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BACKGROUND OF THE INVENTION

5 This section is intended to introduce the reader to aspects of the art that may be related to various aspects of the present invention, which are described and/or claimed below. This discussion is believed to be helpful in providing the reader with background information to facilitate a better understanding of the various aspects of the present invention. Accordingly, it should be understood that these statements are to be read in this light, and not as admissions of
10 prior art.

 The increased speed and capability of computers has had an enormous impact on our society. The Internet, advanced software applications, speed recognition, advances and telecommunications and the many other high speed applications are made feasible only because
15 the performance of silicon-based integrated circuit devices has increased over time. As can be appreciated, faster performance is generally desirable.

 Current integrated circuit devices, such as metal oxide semiconductor (MOS) transistors, are limited by constraints inherent in existing silicon technology. For decades, scientists have
20 been searching for ways to enhance existing silicon technology to speed computer performance. As can be appreciated, any medium that can conduct electricity has some degree of capacitance associated therewith. Technically, a MOS transistor is regarded as a capacitive circuit. This implies that the MOS circuit must completely charge to full capacitance to activate its switching

capability. The process of discharging and recharging the transistor requires a relatively long amount of time when compared to the time it requires to actually switch the voltage state of the transistor's metal layer. The "junction capacitance" of a transistor generally refers to the charge-storing area between the impurities added to a chip's silicon and the impurity-free silicon substrate. Reducing the junction capacitance associated with the transistor will enhance performance of the device by increasing the operating speed.

Silicon-on-insulator (SOI) is a relatively new technology that offers certain advantages over prior techniques. SOI differs from CMOS by placing the transistor's silicon junction area on top of an electrical insulator. The most common insulators employed with this technique are glass and silicon oxide. By placing a thin layer of insulator between the impurities and the silicon substrate, the junction capacitance is greatly reduced or eliminated, thereby enabling the transistor to operate faster. As transistor latency drops, the ability to process more instructions in a given time increases and overall system performance is positively impacted.

Though SOI technology offers certain advantages over existing silicon technology, further size reduction and cost reduction may be desirable. Further, devices having lower leakage currents and stable refresh rates is also desirable. As can be appreciated, improved manufacturability is often desirable, as well.

Fig. 1 illustrates a partial cross-sectional view of a transistor fabricated using silicon-on-insulator (SOI) technology;

Fig. 2 illustrates a partial schematic illustration of an exemplary integrated circuit, incorporating an array of memory cells having transistors fabricated in accordance with embodiments of the present invention; and

Figs. 3-10 are cross-sectional views illustrating exemplary methods of fabricating integrated circuits in accordance with embodiments of the present invention.

DETAILED DESCRIPTION OF SPECIFIC EMBODIMENTS

One or more specific embodiments of the present invention will be described below. In an effort to provide a concise description of these embodiments, not all features of an actual implementation are described in the specification. It should be appreciated that in the development of any such actual implementation, as in any engineering or design project, numerous implementation-specific decisions must be made to achieve the developers' specific goals, such as compliance with system-related and business-related constraints, which may vary from one implementation to another. Moreover, it should be appreciated that such a development effort might be complex and time consuming, but would nevertheless be a routine undertaking of design, fabrication, and manufacture for those of ordinary skill having the benefit of this disclosure.

Turning now to the figures, Fig. 1 illustrates a partial cross-sectional view of a transistor fabricated using silicon-on-insulator (SOI) technology. As previously described, the

development effort might be complex and time consuming, but would nevertheless be a routine undertaking of design, fabrication, and manufacture for those of ordinary skill having the benefit of this disclosure.

5 Turning now to the figures, Fig. 1 illustrates a partial cross-sectional view of a transistor 10 fabricated using silicon-on-insulator (SOI) technology. As previously described, the transistor 10 includes a silicon substrate 12 having an insulator 14, such as an oxide or glass. The gate area (or channel) is formed by disposing a thin layer of silicon 16 on top of the insulator 14 and forming the doped regions 18 and 20 in the thin layer of silicon 16 such that a channel is
10 formed through the thin layer of silicon 16. A thin barrier layer 22, such as an oxide, is disposed over the thin layer of silicon 16 and a conductive layer 24, such as a metal or polysilicon, is disposed on top of the barrier layer 22 and patterned to form a conductive path above the gate area. When current is transmitted to the conductive layer 24, the thin layer silicon 16 forms a conductive channel between the doped regions 18 and 20 through which electricity flows.

15 As can be appreciated, the interface between the doped regions of a transistor and the underlying layer may have an associated junction capacitance. As previously described, a MOS circuit generally uses a relatively large amount of operational time discharging and recharging this capacitance before the transistor is able to conduct since there is a relatively large
20 capacitance associate with the junction between the pure silicon and the doped silicon. However, the present SOI transistor 10 includes an insulator 14 disposed over the silicon substrate 12. Advantageously, the SOI transistor 10 has a negligible capacitance since the insulator 14

provides an efficient barrier. Accordingly, the capacitance associated with the junction 26 is essentially eliminated by incorporating the insulator layer 14, thus allowing the SOI transistor to operate faster since the charging process is virtually eliminated. As will be described further with reference to Figs. 3-8, the notion of providing an insulator 14 to minimize the capacitance at the junctions 26 as in the SOI transistor 10, can be implemented with other technologies, such as shallow trench isolation (STI) technology, to provide improved transistor design for incorporation in ultra large scale integration (ULSI) applications of integrated circuits.

Referring to now to Fig. 2, a partial schematic illustration of an exemplary integrated circuit, such as a memory device, incorporating an array of memory cells having transistors which may be fabricated in accordance with the techniques described herein is illustrated. The memory device 28 may be, for example, a dynamic random access memory (DRAM) device. In the exemplary embodiment, the memory device 28 includes a number memory cells 30 arranged in a grid pattern comprising a number of rows and columns. The number of memory cells 30 (and corresponding rows and columns) may vary depending on system requirements and fabrication technology. Each memory cell 30 includes an access device and a storage device. In the present exemplary embodiment, the access device comprises a field effect transistor (FET) 32 and the storage device comprises a capacitor 34. The access device is implemented to provide controlled access to the storage device. In the exemplary memory cell 30, the FET 32 includes a drain terminal 36 and a source terminal 38. The capacitor 34 is coupled to the source terminal 38. The terminal of the capacitor 34 that is not coupled to the FET 32 may be coupled to a ground plane.

It should be noted that although the above description depicts the terminal of the access device coupled to the capacitor 34 as the source 38 and the other non-gate terminal of the access device as the drain 36, during read and write operations, the FET 32 may be operated such that each of the terminals 36 and 38 operates at one time or another as a source or a drain.

5 Accordingly, for purposes of further discussion it should be recognized that whenever a terminal is identified as a source or a drain, it is only for convenience and that in fact during operation of the FET 32 either terminal could be a source or a drain depending on the manner in which the FET 32 is being controlled by the voltages applied to the terminals 36, 38 and 40.

10 As previously described, the memory array is arranged in a series of rows and columns. To implement the data storage capabilities of a memory cell 30, an electrical charge is placed on the drain 36 of the FET 32 via a bit line (BL). By controlling the voltage at the gate 40 via the word line (WL), a voltage potential may be created across the FET 32 such that the electrical charge at the drain 36 can flow to the capacitor 34. As can be appreciated, by storing electrical
15 charge in the capacitor 34, the charge may be interpreted as a binary data value in the memory cell 30. For instance, for a single-bit storage device, a positive charge above a known threshold voltage may be interpreted as binary "1." If the charge in the capacitor 34 is below the threshold value, a binary value of "0" is said to be stored in the memory cell 30.

20 The bit lines BL are used to read and write data to and from the memory cells 30. The word lines WL are used to activate the FET 32 to access a particular row of a memory cell 30. Accordingly, the memory device 28 includes an address buffer 42, row decoder 44 and column

decoder 46. The row decoder 44 and column decoder 46 selectively access the memory cells 30 in response to address signals that are provided on the address bus 48 during read, write and refresh operations. The address signals are typically provided by an external controller such as a microprocessor or another type of memory controller. The column decoder 46 may also include sense amplifiers and input/output circuitry to further enable data to be read to and from the memory cell 30 via the bit lines BL.

In one exemplary mode of operation, the memory device 28 receives the address of a particular memory cell 30 at the address buffer 42. The address buffer 42 identifies one of the word lines WL of the particular memory cell 30 corresponding to the requested address and passes the address to the row decoder 44. The row decoder 44 selectively activates the particular word line WL to activate the FET's 32 of each memory cell 30 that is connected to the selected word line WL. The column decoder 46 selects the bit line (or bit lines) BL of the memory cell 30 corresponding to the requested address. For a write operation, data received by the input/output circuitry is coupled to the selected bit line (or bit lines) BL and provides for the charge or discharge of the capacitor 34 of the selected memory cell 30 through the FET 32. The charge corresponds to binary data, as previously described. For a read operation, data stored in the selected memory cell 30, represented by the charge stored in the capacitor 34, is coupled to the select bit line (or bit lines) BL, amplified by the sense amplifier and a corresponding voltage level is provided to the input/output circuitry in the column decoder 46.

As can be appreciated, the memory array described in Fig. 2 implements a number of

FETs 32. In accordance with the present exemplary embodiments, the FETs 32 may be fabricated using STI technology. Shallow trenches may be formed in a substrate and filled with an oxide. Cavities may be formed in the field oxide and filled with a conductive material, such as polysilicon, as described further below. In the present exemplary embodiments, the FET 32 includes vertical junctions that are fabricated along the transistor gate edge. As described in detail below, the vertical junctions are formed between the polysilicon and the exposed silicon at the trench edges such that the heavily doped polysilicon will out-diffuse doping elements into the adjacent single crystal silicon advantageously forming a diode extension having desirable properties. Because the vertical junctions are in the single crystal silicon substrate and not the polysilicon layer, the diode area is confined to the transistor edge and thus, does not intersect trench walls, the junction leakage is advantageously low. Further, because the junction landing pad (i.e., the polysilicon) is disposed over the isolation oxide, the transistor cell can be compacted while the field isolation trench width is widened to accommodate the source/drain landing pad contact areas, thereby allowing a better fill margin for the trench. Further, the trench can be made shallower since the diode along the trench walls does not extend far below the surface of the shallow trench. As will be appreciated, the exemplary FETs 32 can be compacted further using self aligned contact (SAC) processing.

Referring now to Fig. 3, a partial cross sectional view of a substrate 50 having STI trenches 52 fabricated therein is illustrated. The substrate 50 may comprise a p-type silicon (Si) substrate, for instance. As described further below, a FET 32 may be fabricated vertically within the trench 52. The trenches 52 may be formed by any one of a number of wet or dry etching

techniques, such as plasma etching, ion beam etching, or reactive ion etching (RIE), for example. The trenches 52 may have a depth in the range of about 0.15 microns to about 0.45 microns, for example. Further, the trenches 52 may have a width in the range of approximately .025 microns to 0.015 microns, for example.

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The structure illustrated in Fig. 3 includes a thin oxide layer 54, such as silicon dioxide (SiO_2) or oxide nitride oxide (ONO), which may be applied or grown on the surface of the substrate 50 by wet or dry oxidation of the semiconductor substrate 50, for instance. The oxide layer 54 may be grown on the surface of the wafer by placing the substrate 50 in a heated chamber and exposing the wafer to oxygen gas, as can be appreciated by those skilled in the art. Alternatively, the oxide layer 54 may be deposited over the substrate 50. The oxide layer 54 is generally a thin layer that forms the gate oxide of the FET 32, as will be illustrated further below.

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The structure illustrated in Fig. 3 also includes an intermediate nitride layer 56, such as silicon nitride (Si_3N_4), that is deposited onto the oxide layer 54 and patterned, as illustrated in Fig. 3. The nitride layer 56 may be deposited to protect the underlying materials during further processing. The nitride layer may comprise various other common insulating materials such as silicon oxide (SiO_2), which may be in combination with the nitride layer 56. The nitride layer 56 may be deposited by chemical vapor deposition (CVD), for example. More specifically, the nitride layer 56 may be disposed using a low pressure chemical vapor deposition (LPCVD).

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The techniques for forming the structure illustrated in Fig. 3 may vary. For instance, in one exemplary embodiment, after the trenches 52 are formed in the substrate 50, the oxide layer 54 may be applied to (or grown on) the surface of the substrate 50, including through the trench 52. Alternatively, the oxide layer 54 and the nitride layer 56 may be disposed over the surface of the substrate 50 before the trenches 52 are formed. Once the oxide layer 54 and the nitride layer 56 are disposed, the trenches 52 may be formed through the nitride layer 56, the oxide layer 54 and the underlying substrate 50. As can be appreciated, if the trenches 52 are formed after deposition of the oxide layer 54, the oxide layer 54 will be removed from the trench 52 during the etch process. Accordingly, a second deposition or growth step may be performed to redeposit or regrow the oxide layer 54 through the trench 52. Once the trench 52 is formed having an oxide layer 54 disposed therein, the trenches 52 are filled with an isolation oxide 58, thereby forming the structure illustrated in Fig. 3. The oxide 58 will provide junction isolation for the FET 32, as illustrated further below.

Once the trench 52 is filled with the isolation oxide 58, the oxide 58 may be patterned such that a shallow cavity 60 is formed along the walls of the channel as indicated in Fig. 4. It should be understood that while the term “cavity” is used to describe the opening formed in the oxide 58, the term is simply used for clarity such that it is easily distinguishable from the trench 52. As can be appreciated, the cavity 60 may also be described as a trench formed in the oxide 58 that extends through the length of the trench 52. In the present exemplary embodiment, the isolation oxide 58 may be etched to form an inverted U-shaped cavity, as illustrated in Fig. 4. As will be illustrated further below, the exposed edge 62 will form a diode junctions for the FET 32

having a low junction leakage based on its proximity to the isolation oxide 58. As used herein, the “exposed edge 62” refers to the edge being essentially free of any film, especially oxides and hydrocarbons.

5 Once the isolation oxide 58 is etched to form the cavity 60 to expose the edge 62, a cleaning process may be implemented to clean the exposed edge 62 to eliminate any films, such as hydrocarbon films, that may be present. After the cleaning process, a conductive material, such as an insitu doped polysilicon (i.e., polysilicon having doping levels in the range of approximately 10^{16} to 10^{22} atoms/ cm^3), amorphous silicon or micro-crystal silicon, for example,
10 may be deposited in the channel by a suitable deposition process, such as chemical vapor deposition (CVD), plasma enhanced chemical vapor deposition (PECVD), or photo enhanced CVD, for example. The conductive material may be deposited in a diffusion furnace or using a single wafer tool, for example.

15 Fig. 5 illustrates the structure formed after deposition of the conductive material, here an N+ doped polysilicon material. Accordingly, the structure illustrated in Fig. 5 includes N+ doped polysilicon 64 disposed in the cavity 60. The polysilicon will be patterned to form the source 36 and drain 38 of the FET 32, as described further below with reference to Fig. 6. Once the polysilicon material 64 is disposed, the structure may be planarized such that the nitride layer
20 56 is flush with the top surface of the polysilicon material 64, as illustrated in Fig. 5. The structure may be planarized using chemical mechanical planarization (CMP) techniques, for instance.

In an alternate embodiment, the polysilicon material 64 may be disposed conformally within the cavity 60, such that a thin layer of the polysilicon material 64 is formed therethrough. The remainder of the cavity 60 may be filled with a compound, such as CuSi_2 , NiSi_2 , TiSi_2 , TiN or W_2N , for example. In another embodiment, the polysilicon material 64 may be replaced completely with a compound, or with a metal that may form a compound through a heat treatment. As will be appreciated, by replacing the polysilicon material 64 with a pure metal, a Schottky barrier may be formed. In this embodiment, the FET 32 may comprise a Schottky barrier transistor having improved gate control and sub-threshold voltage swings. Further, Schottky barrier transistors fabricated in accordance with the present embodiments may provide improved memory cell isolation, reduction in threshold voltage, improvement in drive currents and improved leakage degradation.

After deposition of the conductive material (here the doped polysilicon 64) and CMP, the structure is exposed to a heat treatment. By exposing the heavily doped polysilicon material 64 to a thermal cycle, the doped polysilicon material 64 out-diffuses doping elements into the adjacent single crystal silicon, thereby forming diode extensions for the FET 32, as indicated by the doped regions 68 illustrated in Fig. 6. The lateral diffusion of the polysilicon material 64 may be controlled by controlling the temperature and the time of the thermal cycle such that the depth of the junction is not affected. The exposure time for the thermal cycle is in the range of approximately 20 to 600 seconds and at a temperature in the range of approximately 600°C to 1050°C. Once the out-diffused doped regions 68 are formed in the silicon, the isolation oxide 58

and the polysilicon material 64 are further etched to form the drain 36 and the source 38 and indicated in Fig. 6.

In an alternate exemplary embodiment, the polysilicon material 64 may be etched to form a raised source 38A and drain 36A configuration, as illustrated in Fig. 7. As can be appreciated, the raised source 38A and drain 36A configuration illustrated in Fig. 7 may advantageously provide a lower resistance and faster switching speeds for the FET 32. Those having ordinary skill in the art will appreciate that additional patterning and etching steps may be implemented to form the alternative structure having the raised source 38A and drain 36A of Fig. 7. For instance to complete processing of the structure including the raised source 38A and drain 36A configuration, a dielectric film may be deposited and patterned to isolate the polysilicon material 64 which forms the raised source 38A and drain 36A from the polysilicon material that will be later deposited to form the polysilicon gate 70 (illustrated and described below with reference to Fig. 8).

Returning again to the structure illustrated in Fig. 6, having a source 38 and drain 36 patterned flush with the oxide layer 58, further fabrication of the FET 32 includes a number of deposition, patterning and removal steps. For instance, after the formation of the source 38 and drain 36, the nitride layer 56 may be removed via a chemical etch process such that the gate structures and surrounding materials may be disposed and etched. If the oxide layer 54 is removed during the etch process, the oxide layer 54 may then be regrown to provide the gate oxide for the FET 32. During the regrowth of the gate oxide layer 54, the oxide layer 82 is also

formed over the polysilicon layer 58 (source 38 and drain 36), as illustrated in Fig. 8. Next, the wordline structures implemented to form the gate 40 of the FET 32 may be fabricated. In one exemplary embodiment, the wordlines comprise a polysilicon gate 70 having a silicide material and a nitride cap, such as Si_3N_4 , disposed thereon, illustrated collectively in Fig. 8 as the cap 72.

5 As can be appreciated, the polysilicon gate 70 may comprise other conductive materials, such as tungsten, to enhance conductivity through the polysilicon gate 70. Further, the cap 72 may also comprise various common insulating materials such as silicon oxide (SiO_2). The layers of the cap 72 may be deposited by chemical vapor deposition (CVD), for example. More specifically, the cap 72 may be disposed using a low pressure chemical vapor deposition (LPCVD).

10 Once the wordline layers (i.e., oxide 54, polysilicon gate 70 and cap 72) are disposed, the wordlines may be patterned and etched by a conventional means. Next, a nitride layer may be disposed and etched to form the nitride spacers 74. After formation of the nitride spacers 74, a number of dielectric layers, such as TEOS and BSPG layers, illustrated collectively as dielectric
15 layers 76, may be disposed over the wordline stacks, thereby burying the wordlines. The structure may then be planarized by chemical mechanical planarization (CMP). Next contact holes are formed through the BSPG layers such that openings to the drain 36 and source 38 are formed. Finally, a conductive material, such as a polysilicon plug 80 may be disposed into the holes to provide contacts to the source and drain and metal trace layers (not shown) may be
20 formed on the surface of the dielectric layers 76. The formations of the contact holes may include multiple etch and/or punch steps. For instance, one or more punch steps and/or one or more etch steps, such as a dry etch, may be implemented to etch through the dielectric layers 76

to the underlying source 38 and drain 36. Advantageously, the techniques described herein allow the plugs 80 to be disposed further from the polysilicon gate 70 since the width of the source 38 and drain 36 may be increased. By moving the plugs 80 further from the gate 70, shorting between the plugs 80 and the gate 70 may be reduced.

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For the raised source/drain configuration illustrated in Fig. 7, slightly different processing steps may be implemented. In one embodiment, after formation of the raised source 38A and drain 36A, the nitride layer 56 may be removed via a chemical etch process. Further, the oxide 54 is etched. Next, a dielectric material, such as an oxide or a nitride or high k materials, may be deposited and patterned to surround the raised source 38A and drain 36A. Next, the polysilicon gate 70 (Fig. 8) may be deposited and planarized by a CMP process, for example. Finally, a silicide material and nitride cap may be deposited over the polysilicon gate 70, as previously described.

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As can be appreciated, to provide electrical contact from the underlying wordlines, contact holes (not shown) may also be formed to the underlying wordline. The contact holes may be filled with a conductive material, such as tungsten, to provide a conductive path from the metal traces to the polysilicon gate 70 (i.e., wordline gate 40 in Fig. 2).

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The application of the present techniques of forming cavities within an oxide disposed in a trench may also be implemented to form connections having extended vertical contact regions. Referring briefly to Fig. 4, the cavity 60 has been formed in the P-type silicon substrate 50. To

provide connections along the exposed edge 62, a P+ doped polysilicon may be deposited into the cavity 60, as opposed to the N+ doped polysilicon material 64 implemented to form the transistor junctions, as described above. Further, in some applications, it may be desirable to form connections on one side of the trench 52 (Fig. 3) and to form diode/transistor junctions on the opposite side of the trench 52. The formation of such structures is described briefly with reference to Figs. 9 and 10, below.

As will be appreciated, to facilitate the formation of two structures (i.e, connections and diode/transistor junctions) within a single trench 52, separate cavities may be formed in the isolation oxide and different dopants may be deposited on each side. Referring to Fig. 9, a first cavity 60A is formed in the isolation oxide 58 along one edge of the trench 52. It should be noted that to provide isolation between the cavity 60A and the cavity that will be formed later on the opposite side of the trench 52, the isolation oxide 58 may be patterned and etched such that it is flush with the top surface of the nitride layer 56, as illustrated in Fig. 9. In the present exemplary embodiment, after formation of the first cavity 60A, an N+ polysilicon material, such as phosphorus, may be disposed into the cavity 60A. After deposition of the N+ polysilicon material into the cavity 60A, a similar set of steps may be implemented and a polysilicon material heavily doped with a p-type material, such as boron, may be deposited in similar cavities formed on the opposite side of the trench 52.

Fig. 10 illustrates the structure formed after deposition of both polysilicon materials. Accordingly, the structure illustrated in Fig. 10 includes n-doped polysilicon 64A disposed in a

cavity 60A formed on one side of the trench 52 and a p-doped polysilicon 64B disposed in a cavity 60B formed on the other side of the trench 52. By exposing the doped polysilicon materials 64A and 64B to a thermal cycle, the doped polysilicon materials 64A and 64B will out-diffuse doping elements into the adjacent single crystal silicon, thereby forming either a diode extensions, as with polysilicon material 64A or a connection, as with polysilicon material 64B. Once each of the polysilicon materials 64A and 64B are disposed, the structure may be planarized such that the nitride layer 56 is flush with the top surface of the polysilicon materials 64A and 64B, as previously described with reference to Fig. 5. As will be appreciated, depending on the application, the connections and diode extensions may be patterned and further fabricated to provide any of a number of desirable structures having improved junctions.

While the invention may be susceptible to various modifications and alternative forms, specific embodiments have been shown by way of example in the drawings and have been described in detail herein. However, it should be understood that the invention is not intended to be limited to the particular forms disclosed. Rather, the invention is to cover all modifications, equivalents, and alternatives falling within the spirit and scope of the invention as defined by the following appended claims.